14. [Twice Amended] A circuit comprising:

a die;

a ground node located on the die;

a power supply voltage node located on the die; and

an electronic device having a variable capacitance characteristic and that is permanently coupled between the ground node and the power supply voltage node and capable of providing an asymmetrical response to incremental voltage variations about an operational node voltage at the power supply voltage node.

REMARKS

Applicant has reviewed and considered the office action mailed on April 24, 2002 and the references cited therewith.

Claims 4 and 14 are amended; and as a result claims 4-6, 9, 10 and 14-16 are now pending in the application. Support for the amendments to claims 4 and 14 is found at page 4, lines 11 and 20.

§112 Rejection of the Claims

Claims 4-6 and 14-16 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 4, as amended, recites "wherein the transistor *has a variable capacitance characteristic* that is capable of decreasing noise signals above an absolute value of an operating voltage value at the voltage node and increasing noise signals below the absolute value of the operating voltage value." (emphasis added) Applicant respectfully submits that the "variable capacitance characteristic" renders claim 4 not indefinite thereby obviating the indefinite rejection.

As to whether the claimed function occurs, applicant respectfully submits that Figure 1C of the application demonstrates that the function occurs for an embodiment of applicant's. Furthermore, for circuits other than applicant's, it may be established whether the claimed

function occurs by measuring the properties of a particular device in a laboratory. Hence, claim 4, as amended, is not indefinite. Therefore, applicant requests withdrawal of the rejection and reconsideration and allowance of claim 4.

Claims 5-6 are dependent on claim 4. For reasons analogous to those stated above and elements in the claims, applicant respectfully submits that claims 5-6 are not indefinite. Therefore, applicant requests withdrawal of the rejections and reconsideration and allowance of claims 5-6.

The grounds of rejection of claim 14 are similar to the grounds of rejection of 4. Claim 14, as amended, recites "an electronic device having a variable capacitance characteristic and that is permanently coupled between the ground node and the power supply voltage node." Applicant respectfully submits that the arguments provided above with respect to claim 4 are applicable to claim 14, as amended. Thus, claim 14, as amended, is not indefinite. Therefore, applicant requests withdrawal of the rejection and reconsideration and allowance of claim 14.

Claims 15-16 are dependent on claim 14. For reasons analogous to those stated above and elements in the claims, applicant respectfully submits that claims 15-16 are not indefinite. Therefore, applicant requests withdrawal of the rejections and reconsideration and allowance of claims15-16.

§102 Rejection of the Claims

Claims 9-10 and 14-16 were rejected under 35 U.S.C. § 102(e) as being anticipated by Sin (U.S. Patent No. 5,130,564). Applicant traverses the rejections of claims 9-10.

Claim 9 recites "a transistor coupled between the high power supply voltage node and the low power supply voltage node. . . ." In contrast, Sin in FIG. 5A shows a variable capacitor (VCL) coupled between voltage nodes V_0 and V_R. A variable capacitor is a two terminal device, as shown in FIG. 6B of Sin, while a transistor is a three terminal device. So, the variable capacitor shown in Sin is not a transistor. Hence, since the variable capacitor of Sin is not a transistor, Sin does not teach "a transistor coupled between the high power supply voltage node and the low power supply voltage node" as recited in claim 9. Thus, since Sin does not teach each of the elements recited in claim 9, the office action fails to state a *prima facie* case of

anticipation with respect to claim 9. Therefore, applicant requests withdrawal of the rejection and reconsideration and allowance of claim 9.

Claim 10 is dependent on claim 9. For reasons analogous to those stated above and the elements in the claim, applicant respectfully submits that claim 10 is not anticipated by Sin. Therefore, applicant requests withdrawal of the rejection and reconsideration and allowance of claim 10.

Claim 14, as amended, recites "an electronic device *having a variable capacitance characteristic and that is* permanently coupled between the ground node and the power supply voltage node and capable of providing an asymmetrical response to incremental voltage variations about an operational node voltage at the power supply voltage node." (emphasis added) In contrast, Sin in FIG. 2A shows a capacitive load (CL) coupled between a node common to transistors PM and NM and a ground node. FIG. 2A also shows the CL as switchable between the node common to the transistors PM and NM and power supply voltage node V_{CC}. Hence, since the CL does not have a variable capacitance characteristic (CL is shown as a fixed capacitor in FIG. 2A) and the CL is not is not permanently coupled between the ground node and V_{CC}, Sin does not teach "an electronic device having a variable capacitance characteristic and that is permanently coupled between the ground node and the power supply voltage node and capable of providing an asymmetrical response to incremental voltage variations about an operational node voltage at the power supply voltage node" as recited in claim 14, as amended. Thus, since Sin does not teach each of the elements recited in claim 14, as amended, the office action fails to state a *prima facie* case of anticipation with respect to claim 14, as amended. Therefore, applicant requests withdrawal of the rejection and reconsideration and allowance of claim 14.

Claims 15-16 are dependent on claim 14. For reasons analogous to those stated above and the elements in the claims, applicant respectfully submits that claims 15-16 are not anticipated by Sin. Therefore, applicant requests withdrawal of the rejection and reconsideration and allowance of claims 15-16.

§103 Rejection of the Claims

Claims 4-6 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Freyman, et al. (U.S. Patent No. 5,828,251) in view of Nakai (JP 10242414A).

The office action must provide specific, objective evidence of record for a finding of a suggestion or motivation to combine reference teachings and must explain the reasoning by which the evidence is deemed to support such a finding. *In re Sang Su Lee*, 277 F.3d 1338, 61 U.S.P.Q.2d 1430 (Fed. Cir. 2002). Since the office action fails to address this issue and since neither Freyman et al. nor Nakai provide a teaching, suggestion or motivation to combine the references, applicant respectfully submits that the references are not combinable and thus the office action fails to state a *prima facie* case of obviousness with respect to claims 4, 5 or 6.

Claim 4, as amended, recites "*the transistor operating in the depletion mode*, the gate comprising a p-type polysilicon, wherein the transistor *has a variable capacitance characteristic and* is capable of decreasing noise signals above an absolute value of an operating voltage value at the voltage node and increasing noise signals below the absolute value of the operating voltage value." (emphasis added) In contrast, neither Freyman et al. nor Nakai teach or suggest a transistor including the elements included in claim 4, as amended. The function of the Freyman et al. transistor 202 of Fig. 2 is referred to at column 2, line 9 as " the capacitor formed by transistor 202 is charged through transistor 201. . . ." Thus, Freyman teaches only the use of a charging capacitor and not a capacitor operating in the depletion mode or a transistor having a variable capacitance characteristic, as recited in claim 4, as amended. And Nakai in the abstract teaches only "using p-type polysilicon as gate electrodes," but fails to teach a capacitor operating in the depletion mode or a transistor having a variable capacitance characteristic as recited in claim 4, as amended. Thus, the references fail to teach one of the elements of claim 4, so the office action fails to state a *prima facie* case of obviousness with respect to claim 4.

Claims 5 and 6 are dependent on claim 4. For reasons analogous to those provided above and elements in the claims, applicant respectfully submits that the office action fails to state a *prima facie* case of obviousness with respect to either claim 5 or claim 6.

Therefore, applicant requests withdrawal of the rejections and reconsideration and allowance of claims 4, 5 and 6.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at 612-371-2109 to facilitate prosecution of the application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

RAJENDRAN NAIR ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 371-2109

Date June 24, 2002 By Danny Padys

Danny J. Padys
Reg. No. 35,635

CERTIFICATE UNDER 37 C.F.R. 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Box AF, Commissioner of Patents, Washington, D.C. 20231, on this 24 day of June, 2002.

Name June Brocksch Signature